IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In Re the Application of: | |
| TAE-WOO JUNG, ET AL. | Art Group: |
| Application No.: | Examiner: |
| Filed: | |
| For: **METHOD FOR FABRICATING SEMICONDUCTOR DEVICE HAVING TRENCH TYPE DEVICE ISOLATION LAYER** | |

**INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Utility Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: December 30, 2003

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Substitute for form 1449A/PTO

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(use as many sheets as necessary)*

| Sheet | 1 | of | 1 |
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| Complete if Known | |
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| Application Number | |
| Filing Date | |
| First Named Inventor | Tae-Woo JUNG |
| Art Unit | |
| Examiner Name | |
| Attorney Docket Number | 51876P542 |

## U.S. PATENT DOCUMENTS

| Examiner Initials* | Cite No.[1] | Document Number: Number - Kind Code[2] *(if known)* | Publication Date or Issue Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|
| | | US-6,444,540 B2 | 09-03-2002 | Kawada et al. | |
| | | US-6,500,727 B1 | 12-31-2002 | Chen et al. | |
| | | US-6,218,309 B1 | 04-17-2001 | Miller et al. | |
| | | US-6,579,801 B1 | 06-17-2003 | Dakshina-Murthy et al. | |
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## FOREIGN PATENT DOCUMENTS

| Examiner Initials* | Cite No.[1] | Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] *(if known)* | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear | T[6] |
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| Examiner Signature | | Date Considered | |
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08A (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 08/11/2003.

Send To: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

# Information Disclosure Statement

New U.S. Patent Application for
METHOD FOR FABRICATING SEMICONDUCTOR DEVICE HAVING TRENCH TYPE DEVICE ISOLATION LAYER
Our Ref. No.: P03H3019/US/cj

Reference No.:

(1) US Patent No. 6,444,540
(2) US Patent No. 6,500,727
(3) US Patent No. 6,218,309
(4) US Patent No. 6,579,801